

An Alternative Current-Error Based Control for VSC Integration to Weak Grid

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Abstract— An enhanced current control strategy is proposed for voltage source converters for the integration to weak grids. The control derives from the current-error based vector control. By implementing simple close-loop compensations of both angle and magnitude inputs to the pulse width modulation, the damping of vector control in the weak grid can be significantly improved hence able to deliver full rated power to very weak grid. Due to the presence of the current loop, the fault-ride-through capability can be maintained with no need for mode switching. A comprehensive frequency domain model is employed to analyze the stability. Time domain simulations are further carried out to validate its effectiveness and robustness of integrating to the weak grid with fault-ride-through capability.

Index Terms -- Current Control, Stability, Fault-ride-through, Voltage Source Converter, Weak Grid.

I. INTRODUCTION

The type of power electronics converter called Voltage Source Converter (VSC) is gradually penetrating the power grid as well as the traditional synchronous generators nowadays. As the interface between the traditional AC power system and emerging power grid elements, such as wind turbine [1], Photovoltaic (PV) array [2], battery energy storage [3], High Voltage DC (HVDC) link [4], the overall rating of VSC is growing higher and higher.

One of the consequences brought about by the growing penetration of VSC is that the grid is becoming relatively “weak” [5]. It is due to not only the reduction of physical inertia but also the growing rating and the distance between VSC and those centralized power plants with physical inertia [6]. Traditionally, the grid connection is considered to be “weak” when the Short Circuit Ratio SCR is as low as 3 and “very weak” when SCR is lower than 1.5. Two factors are considered for low SCR – a large VSC rating and a long delivery distance to the voltage sources with inertia [7].

Vector control is prevalently implemented for VSC integration to the power grid and proved to be able to effectively

harness the fault current under most severe grid voltage sags [8]. However, it is also found that with conventional current-error based vector control, low frequency oscillations may be triggered at very weak grid [9]. It happens when the power to be delivered rises closed to its rated value. And it is found that the weaker the grid is, the less amount of power can be delivered.

In order to cope with the instability of VSC integration in weak grid, various methods have been reported. On type of methods are those based on the virtual synchronous machine [10]-[12], which mimics the power-angle behavior of a synchronous machine to get the power fully delivered from the weak ends. The consequent problem is that such control strategies impose no current loop, which is difficult to completely harness the fault current during voltage dip. Thus, a current-error based control has to be employed as a back-up option so as to be switched to when there is a fault [12]. A current based hysteresis shall be used for such switching scheme. Unfortunately, the switching can cause issues as it is very difficult to determine the hysteresis threshold to keep a balance between investments and the performance.

Another type of control strategy seeks to enhance the damping of vector control so as to maintain the excellent fault-ride-through capability of current-error based vector control [13]-[15]. So far, the reported method is complicated for implementation [13], [14] or is changing the well-established current control scheme internally [15].

As the low frequency oscillation is considered to be lack of damping, a simple compensation method is proposed in this paper. The proposed method is based on conventional vector control strategy. By adding angle and magnitude compensations to the inputs of the Pulse Width Modulation (PMW) of the VSC, the compensation can be easily implemented with no internal change to the well-established current regulation of vector control. The paper is organized as follows: the principles of the proposed control strategy are introduced in Section II; a frequency domain analysis is carried

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out in Section III; Section IV covers the time domain studies and the conclusion is drawn in Section V.

II. PRINCIPLES OF THE PROPOSED CURRENT-ERROR BASED VSC CONTROL IN WEAK GRID

A. Modelling of VSC connecting to Weak Grid

For the study of dynamics, the VSC integration to the weak grid can be modelled as an instantaneously controlled voltage source connecting to infinite AC bus via filter impedances and the line impedances, which is shown in Fig. 1.

As is shown in Fig. 1, R_1 and L_1 are the resistive and inductive impedance of the reactor connecting to a 3-phase bridge. C and L_{tx} are the VSC filter capacitance and leakage inductance of VSC transformer, respectively. R_2 and L_2 are the resistive and inductive impedances of the grid Thevenin Equivalent, which includes both the transmission lines and possible VSC transformer. The converter modulation voltage is denoted as V_{conv} whereas the capacitor voltage V_c .

B. Control Strategy with Damping Compensation

As is well documented by industry and academia, the traditional vector control cannot enable fully rated power delivery from the weak grid. In this paper, a modified control

Considering the real power output to the grid is linear to the d-axis current in rotating reference frame; whereas in stationary polarity reference frame, the power is determined by the sinusoidal function of the power angle which is the angular difference between the converter modulation voltage vector and the capacitor vector, a closed loop compensation can therefore be established with the corresponding linear relationship between the sinusoidal function of power angle and d-axis current. If only small signal is considered, the differential of the sinusoidal function can be linearized as the differential of the VSC output voltage angle. As a result, the relationship between the differentials of VSC output angle and the d-axis current can be considered as linear. Therefore, a closed-loop compensation can be established based on such relationship as shown in the dotted box of Angle Compensation. A proportional regulator is employed to feed the output of angle compensation as a super-imposing component for the input of PWM block.

strategy is proposed based on the conventional vector control, which is illustrated by Fig. 2. As shown, angle compensation and magnitude compensation, which are denoted in the dotted boxes, are added to the conventional vector control strategy.

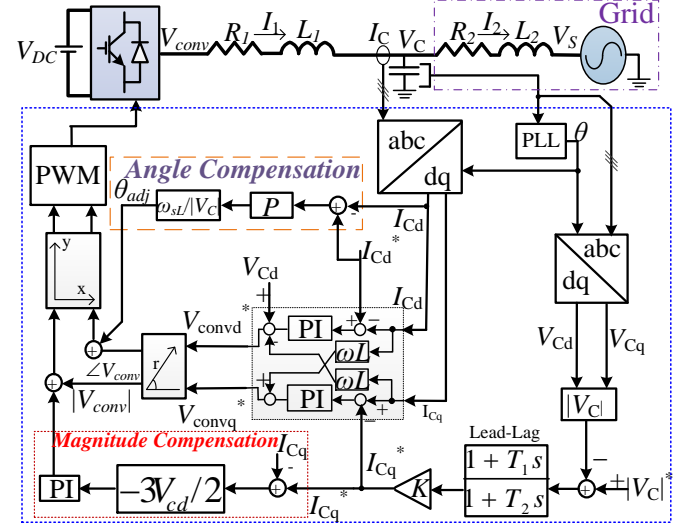


Fig. 1. Schematic of the benchmark system and proposed VSC control.

Similarly, considering the approximate linear relationship of reactive power against q-axis current and the linear relationship between the VSC output voltage against the reactive power, the relationships of the differentials of the q-axis current and output voltage magnitude can be considered linear as well. Similar to the angular compensation, a closed-loop compensation is proposed as shown in Fig. 1 as the Magnitude Compensation. And magnitude compensation is again fed as a super-imposing component of the magnitude of the modulation signal.

The advantage of the compensation is that it does not change the internal current control of conventional vector control.

III. FREQUENCY DOMAIN ANALYSIS

A. The analytical model in frequency domain

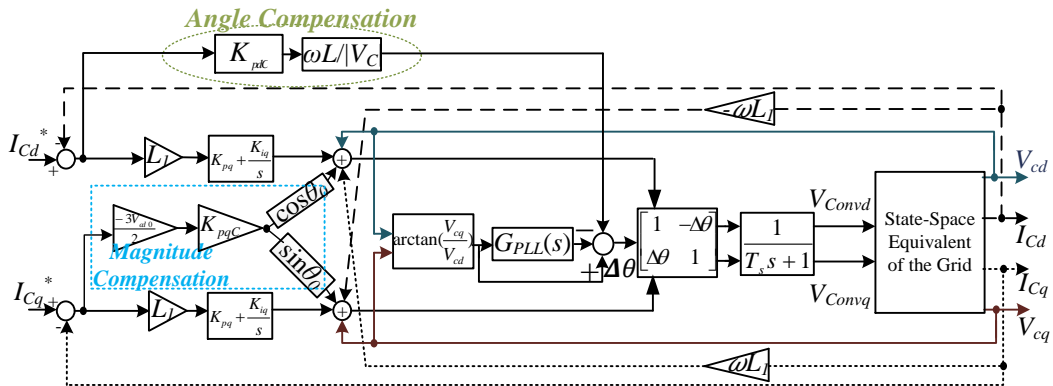


Fig. 1. Schematic of the proposed VSC control.

A frequency domain analytical model is established based on the proposed control strategy of Fig. 1, which is shown in Fig. 2. As is shown in Fig. 2, the proportional and integral gains of angle compensation represented by K_{pdC} and K_{idC} , respectively the gain for the magnitude compensation is represented by K_{pqC} ; V_{cd0} and θ_0 refer to the values of the operational capacitor voltage and angle. K_{pd} , K_{id} , K_{pq} , K_{iq} are the PI controller parameters for d- and q-axis.

The dynamic of Phase-Locked-Loop (PLL) is represented by a process of $G_{PLL}(s)$

$$r \quad (9)$$

where K_p and K_i are the proportional and integral gains respectively. The process of $\arctan(V_{cq}/V_{cd})$ can be linearized as with Taylor Expansion at the analytical point of (V_{d0}, V_{q0}) as

$$\arctan \frac{V_q}{V_d} \approx \frac{V_{q0}}{V_{d0}} + \frac{1}{1 + \frac{V_{q0}^2}{V_{d0}^2}} \left(\frac{V_q}{V_d} - \frac{V_{q0}}{V_{d0}} \right) \quad (10)$$

The main circuit of a converter is considered to be connecting to the grid, which can be modelled as a state-space model [16] as

$$\dot{x} = Ax + Bu \quad (11)$$

and

$$x = [i_{Cd}, i_{Cq}, V_{Cd}, V_{Cq}, i_{2d}, i_{2q}]^T \quad u = [V_{sd}, V_{sq}, V_{convd}, V_{convq}]^T \quad (12)$$

$$A = \omega_b \begin{bmatrix} -\frac{R_2}{L_2} & \omega & -\frac{R_2}{L_1} & 0 & 0 & 0 \\ \omega & -\frac{R_2}{L_2} & 0 & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C} & 0 & 0 & -\omega & -\frac{1}{C} & 0 \\ 0 & \frac{1}{C} & \omega & 0 & 0 & -\frac{1}{C} \\ 0 & 0 & \frac{1}{L_2} & 0 & -\frac{R_2}{L_2} & \omega \\ 0 & 0 & 0 & \frac{1}{L_2} & -\omega & -\frac{R_2}{L_2} \end{bmatrix}; \quad (13)$$

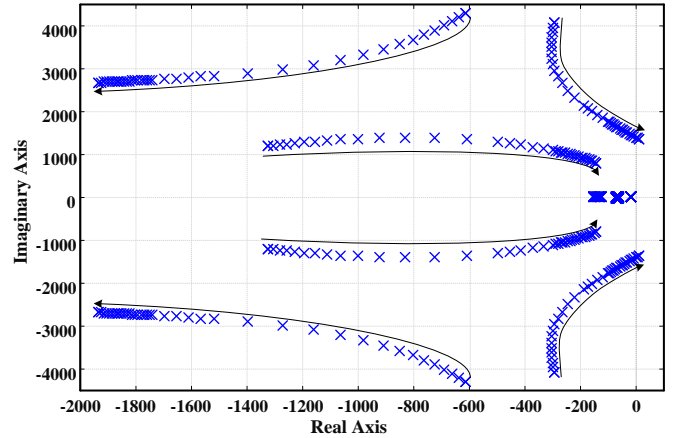
$$B = \omega_b \begin{bmatrix} 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 \end{bmatrix}$$

B. System analysis

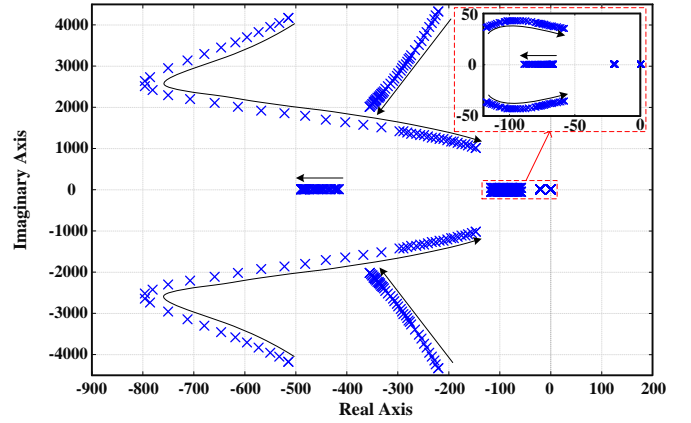
With the frequency domain model shown in Fig. 2, a frequency model analysis can be carried out with root locus analysis shown in Fig. 3. The parameters used are listed in Table I.

TABLE I SYSTEM PARAMETERS

Transformer Inductance	l_{tx}	0.1 pu
Transformer ratio	N_{tx}	0.69/33kV
VSC nominal voltage	V_n	690 V
Reactor inductance	L_1	0.2 pu
Filter Capacitance	C_f	0.1 pu
Current controller proportional gains	$K_{pd} = K_{pq}$	$141 \pi L_1$
Current controller integral gains	$K_{id} = K_{iq}$	$10000 \pi^2 L_1$
PLL proportional gain	K_p	178
PLL Integral gain	K_i	3947
Voltage controller droop gain	K	15
Short Circuit Ratio	SCR	1
Angle compensation proportional gain	K_{pdC}	0.2
Magnitude compensation integral gain	K_{iqC}	4
Magnitude compensation proportional gain	K_{pqC}	0.2
Lead-lag filter nominator time constant	T_1	0.004s
Lead-lag filter denominator time constant	T_2	0.02s



(a) Conventional control (with SCR from 10 towards 1)



(b) The proposed control (with SCR from 10 towards 1)

Fig. 3. Root locus analysis.

As is shown in Fig. 3 (a), with the conventional control strategy, when the SCR becomes very small (SCR = 1 in particular), the system tends to be unstable as the roots reach the right plane, which demonstrates that the conventional control is unable to deliver full power when the grid is very weak. By adding the angular and magnitude compensation, the proposed alternative control can effectively push the poles towards to the left plane, which is shown in Fig. 3(b).

IV. CASE STUDIES

In order to further validate the proposed control, time domain case studies are carried out in this section.

A. Current Ramp Test

In order to test the capability of delivering fully-rated power, a ramp test is carried out in Fig. 4. As is shown in Figs. 4 (i) and (ii), a ramp power order is triggered from Time = 0.1 s, with a ramp rate of 6.6 p.u./s. For the conventional control in Fig. 4(i), the power and voltage start to oscillate when the order reaches around 0.65 p.u. due to lack of damping; whereas it can be seen in Fig. 4(ii) that the fully-rated power can be delivered throughout the ramping-up. At Time = 0.5 s, the ramping-down order is triggered. Similarly, the power ramps down smoothly. Throughout the process, the voltage is maintained within a reasonable variation of 2%. It can also be found in the test that the angular compensation is less than 0.001 rad in this process which means that angle is not shifted in the process so the current of d- and q- axis are still well decoupled according to the capacitor voltage.

B. Step Test

To further test the performance of the proposed control, a step response is carried out, which is shown in Fig. 5. In order to test the performance in an adverse condition, the system starts with a real power delivery of 0.95 p.u.. A step order of 0.05 p.u. is given at Time = 0.1 s. It can be seen that after oscillation of 0.1 second, the power converges at 1 p.u., which proves that the proposed control has a good stability at the very weak grid.

C. Low-voltage-ride-through Test

Comparing with virtual synchronous control, the main advantage of the proposed control is that it can limit the current after a fault. In order to test the performance of the proposed control, a most adverse 3-phase short fault is considered to be closely at the grid connection point.

As is shown in Fig. 6, the simulation is carried out when SCR = 1 and the VSC is delivering rated power from Time = 0 s. It is assumed that DC side power can be well harnessed. As shown in Fig. 6, a 3-phase fault occurs at Time = 0.1 s. The fault is considered to be closely located at the connection point and the capacitor voltage drops to almost 0 V. It can be seen that the overall current rise up immediately after the fault; however, the sudden overshoot of the current magnitude is limited to less than 1.4 p.u. and then is confined to less than 0.3 p.u. during the fault. After 100 ms, the fault is cleared. The fault current is trying to follow a pre-defined curve and return to the pre-fault values.

From Fig. 6, it can be clearly seen that the proposed control is capable of harnessing the fault current during a 3-phase fault without control mode switching.

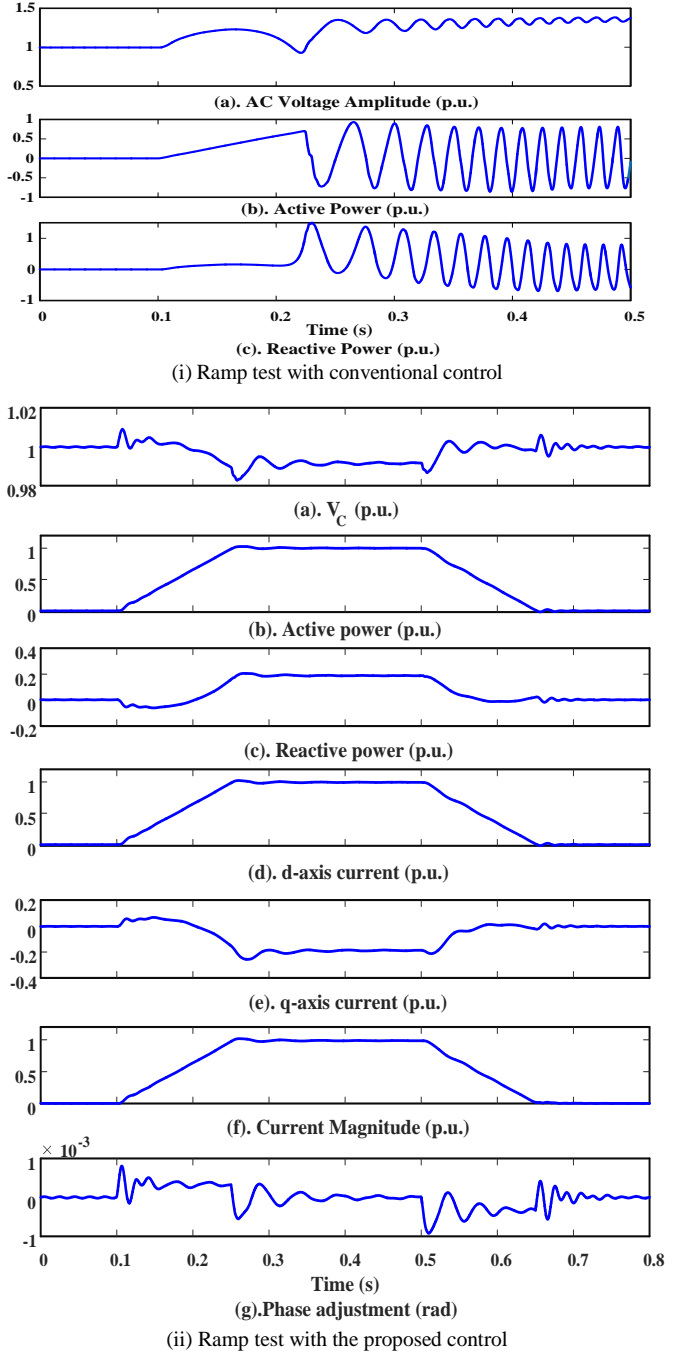


Fig. 4. Ramp test with the proposed control

V. CONCLUSIONS

An enhanced vector control strategy is proposed for VSC integration to the weak grid in this paper. The proposed control method is able to deliver full power from the weak grid while still can take advantage of the presence of current loops.

The frequency domain analysis shows that the proposed d-axis current error based angular compensation and q-axis current error based magnitude compensation, which is fed into the PWM reference values, can effectively improve the system damping at very weak grid.

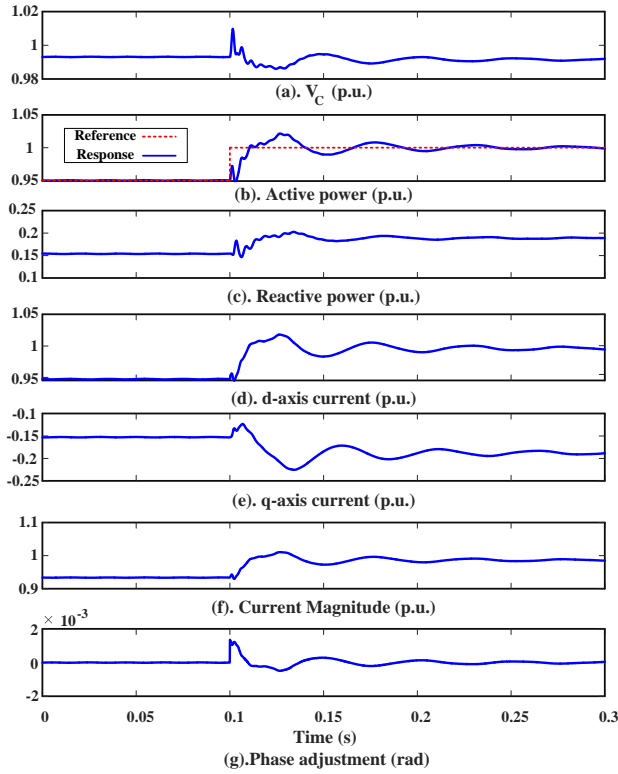


Fig. 5. Step test with the proposed control

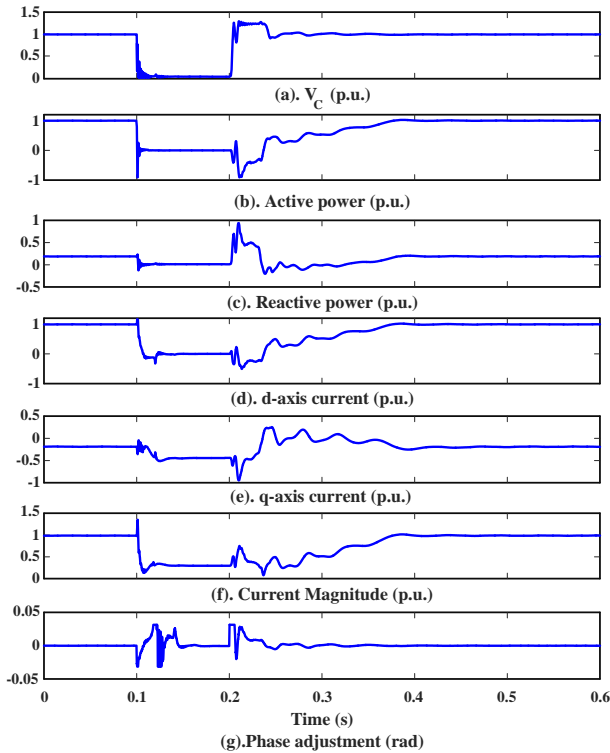


Fig. 6. Low-voltage-ride-through test for the proposed control

The proposed compensation can be further validated by time domain simulations that the proposed control can enable full power delivery at steady state ramp operation, power step and the fault-current limiting during a significant transient of 3-phase short circuit at the connection point.

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